The Korean Intellectual Property Office (KR)
Registration patent official report (B1)

(51) Int.Cl.
G11C 11/406 (2006.01)

(11) Publication No	10-1998-0042579 10-0537256
(43) Publication Date	1998-08-17 2006-07-10
(21) Application No	10-1997-0061007
(22) Application Date	1997-11-19
(30) Priority Claims	96-308280 1996-11-19 Japanese (JP) 97-167630 1997-06-24 Japanese (JP)
(74) Agent	Yeong-Cheol Kim
(72) Inventor	SiBaYaMa AKiNoRi YAMADA,Toshio
(73) Right Holder	MATSUSHITA ELECTRIC INDUSTRIAL CO.. LTD.

Examiner : Byeong-Il Ahn

(54) SEMICONDUCTOR MEMORY.

Abstract

1 The present invention relates to the memory including the semiconductor memory, and especially, DRAM and DRAM and the memory of being useful in case the logic circuit mixes, and even if it has the current leakage of a little from the memory cell, data retention time is long secured and the long refresh cycle period is to be gotten. Memory cell (11~15 and 2) are connected to the word line (WL). And the memory cell (11~15) for the information is inputted to the input terminal of the sense amplifier (SA1~5) one side via the bit line (bit1~5). In the other memory cell (2), the suitable reference information is memorized in the reference potential of the information read. It is common to each input terminal on the other side of the sense amplifier (SA1~5) via the bit line (bit7) and this reference information is inputted. Therefore, the electric potential of the signal charge memorized in the memory cell (11~15) for each information is degraded due to the leakage current. Still, the time is extended and since the electric potential of the signal charge memorized in the memory cell (2) which thus additionally memorizes the information of the reference potential being degraded with the leakage current, the number of the electric potential difference between both sides reaches the sense limit data retention time can be long maintained.

Representative Drawing(s)

Fig. 1

Description

Brief explanation of the drawing

2 Fig. 1 is a view of whole configuration showing the first preferred embodiment of the present invention.

3 Fig. 2 is a drawing showing the changed example according to the first preferred embodiment of the present invention.

4 Fig. 3 is an illustrative view for illustrating the enhancement effect of data retention time according to the first preferred embodiment of the present invention.

Fig. 4 is a view of whole configuration showing the second preferred embodiment of the present invention.

Fig. 5 is a detail view of the main part of the second preferred embodiment of the present invention.

Fig. 6 is an operation description of the second preferred embodiment of an invention.

Fig. 7 is an operation state diagram of the control transistor with the classified by contents of a control as to the semiconductor memory of the second preferred embodiment of the present invention.

Fig. 8 is a view of whole configuration of the third preferred embodiment of the present invention.

Fig. 9 is a detail view of the main part of the third preferred embodiment of the present invention.

Fig. 10 is an illustrative view for illustrating the effect of the correction method according to the third preferred embodiment of the present invention.

Fig. 11 is an illustrative view for illustrating the effect of the floating wiring and configuration according to the fourth preferred embodiment of the present invention.

Fig. 12 is an illustrative view for illustrating the enhancement effect of data retention characteristic in the semiconductor memory according to the fourth preferred embodiment of the present invention.

Fig. 13 is a configuration diagram of the conventional redundancy circuit.

Fig. 14 is a configuration diagram of the fifth preferred embodiment of the present invention.

Fig. 15 is a configuration diagram of the redundancy circuit of the fifth preferred embodiment of the present invention.

Fig. 16 is a configuration diagram of the sixth preferred embodiment of the present invention.

Fig. 17 is a configuration diagram of the dynamic configurable logic of the sixth preferred embodiment of the present invention.

Fig. 18 is an operation description of the sixth preferred embodiment of the present invention.

Fig. 19 is a configuration diagram of the memory cell of the seventh preferred embodiment of the present invention.

Fig. 20 is a configuration diagram of the conventional memory cell.

Fig. 21 is a drawing showing the changed example of the memory cell according to the seventh preferred embodiment of the present invention.

Fig. 22 is a schematic configuration diagram of the micro type memory module of the eighth preferred embodiment of the present invention.

Fig. 23 is a configuration diagram of the memory core of the conventional DRAM.

Fig. 24 is an illustrative view of data retention time characteristic of the memory core of the conventional DRAM.

Fig. 25 is a concrete internal structure diagram of data processing block in the ninth preferred embodiment of the present invention.

Fig. 26 is a concrete internal structure diagram of data processing block in the 10th preferred embodiment of the present invention.

Fig. 27 is a whole schematic configuration diagram of the computer system in the eleventh preferred embodiment of the present invention.

Fig. 28 is an internal structure diagram of the shared memory having data handling function in the eleventh

preferred embodiment of the present invention.

The description of reference numerals of the main elements in drawings

2: reference memory cell 11~ 16: information memory cell.

WL: word line bit1~ bit8: bit line.

SA1? SA5: sense amplifier 54: intermediate value generation circuit.

PRB1, PRB2: local probe 56: register SRAM.

Gbit1? Gbit1: global bitline 60, 61: preamp part.

Ccall, Ccal2: the condenser for a correction CW: bit line entry switch.

CL1, CL2: transistor switch M1: floating wiring.

71: redundancy circuit 74: serial transfer circuit.

75: variable coding region 76: fixing coding region.

80: memory core 81: register group.

85a, 85b: dynamic configurable logic 86: general purpose register.

90: unit logic 91: channel wire portion.

92: programmable switch element 92a: *** MOSFET.

c: condenser 92b: MOSFET for the load.

92c: CELP boot dragon MOSFET 102: storage node.

103: dielectric film 104: plate electrode.

A: first memory array B: second memory array.

130, 130': data processing block 150: switching matrix S heat.

PL: programmable logic 149: first word line group.

151: first memory cell group 152: second word late king.

153: second memory cell group 154: third word late king.

155: third memory cell group 160: second multi-bit data bus.

180: second multi-bit register 179, 181: memory bus.

MM:shared memory(the semiconductor device having data handling function)

Details of the Invention

Purpose of the Invention

The Technical Field to which the Invention Belongs and the Prior Art in that Filed

The present invention relates to the memory including the semiconductor memory, and especially, the DRAM (dynamic random access memory) and DRAM and the memory core which is useful in the mixed loading of the logic circuit.

56 A recent, and a memory, especially, the enlargement of the DRAM degree of integration are every year enlarged. Therefore, the refresh cycle period long in order not to reduce the usable period of the memory is required. It has the tendency that it is difficult to the ability value which accordingly is required from data retention time be high required and realize this as the process device.

57 Hereinafter, the ability value of data retention time of the memory is described referring to Fig. 23.

58 Fig. 23 is an organization outline drawing of the conventional DRAM. As to Fig. 23, the Cs the memory capacity (storage capacitor) of the memory cell, WL1 , and WL2 the word line, a bit , and a xbit the bit line and complementary bit line , and Vpre the bitline precharge voltage , and Ppre the pre charge control line , and SA are the sense amplifier.

59 The operation of the conventional DRAM decides to be simply illustrated. Firstly, the pre charge control line (Ppre) is high-leveled. The bit line and complementary bit line (bit, xbit) are set up as the precharge level (Vpre). Next, the pre charge control line (Ppre) is low level. The electric potential of the word line (WL1) and then rises and the miniature potential is generated with the signal charge accumulated in the memory cell (Cs) in the bit line (bit). The miniature potential is amplified in the sense amplifier (SA).

60 The Cs (Vcs-Vplate) +Vpre*CB= Cs (Vr'-Vplate) +Vr'*CB it has the memory electric potential of the memory cell (Cs) at the just before as the Vcs that the electric potential of the word line (WL1) is risen.

62 It becomes. Here, as to vplate, the cell plate voltage , and CB the capacity of the complementary bit line and bit line , and Vr' are the settled bit line potential after reading the electric charge from the memory cell.

63 The micro voltage (Delta-v), which the sense amplifier (SA) amplifies from the equation is the Delta-V= Vr'-Vpre=a * (Vcs- Vpre)

65 a=Cs/(Cs+CB)

66 It becomes.

67 In case the micro voltage (Delta-V) is greater than the discrimination fhreshold resolution (?sa) of the sense amplifier (SA), it is exact for the first time, data are read. For example, in case data of "1" is entered and data reads, the power supply voltage is to Vdd

68 The voltage of the Delta-V=a * (Vdd-Vpre) =0.2 * (3.3-1.65) =330mV is generated. And data of "O" is entered and the voltage reads.

70 The voltage of the Delta-V=a * (0-Vpre) =0.2 * (0-1.65) =-330mV is generated. And here, it was done by an a=0.2, the Vdd= 3.3V, and the Vpre=Vdd / 2.

71 An ordinarily, and the discrimination fhreshold resolution (Vsa) of the sense amplifier (SA) are about 50mV. Therefore, an ordinarily, and the discrimination fhreshold resolution (Vsa) of the sense amplifier (SA) without any problem accurately operate in case of above statement.

72 Next, the case in which the voltage which has the leakage current and written in the memory cell (Cs) is not like that outputted can be considered. From a * (Vcs1L-Vpre) =Vsa "1" was written.

74 It consists of 0.2 * (VcslL-1.65) =0.05.

75 In VcslL=1.9V, the malfunction is initiated. The time is the ability value of data retention time the number reaches a limit. This relation is shown in Fig. 24.

Technical challenges of the Invention

76 Although the object of the present invention has the current leakage of a little, it long secures data retention time and it gets the long refresh cycle period. It prevents the degradation of the and, data retention time is short, caused production yield. The degradation further more is to realize the low cost of the process whole.

▸ Structure & Operation of the Invention

77 The present invention for the object achieving does that it fits the reference potential at the sense amplifier with the voltage drop caused by the leakage current at the memory cell and the reference potential drops.

78 The sense amplifier it is the reference information corresponding to the reference potential of the information read from the memory cell for the information in the other memory cell as described above it is made of the capacity and transistor and the first semiconductor memory of the present invention includes the memory cell for the information performing moreover, the read operation of the information, the word line accessing the memory cell, and the memory cell of the other *** and the memory cell connected to the word line having the word line and identity or the same address for the object achieving described in the above are characterized that the used information is remembered.

79 And provided is the semiconductor memory, in which the number of memory cell for the information is more than the number of the other memory cell over 1.

80 Moreover, the semiconductor memory is characterized by including the reference potential generating circuit generated around the reference potential based on the information which is accumulated "1" and "0" information in 2 memory cells of the other memory cell.

81 And the semiconductor memory is characterized by including the reference potential generating circuit generated around the reference potential based on the accumulated multi-value information in the other memory cell more than 3 the pluridentate information is memorized in the other memory cell more than the memory cell for the information more than 3 and 3.

82 Moreover, it is characterized that as to the semiconductor memory, the first memory cell group having the memory cell for the information is nearly equally divided into 2. The second memory cell group having the other memory cell memorizing the reference information is arranged in the interval.

83 And the second semiconductor memory of the present invention is characterized that the information is remembered. The memory cell array having the memory cell in which a read and writing operation of the information are possible is included with plurality. Simultaneously, it is connected to the memory cell of each memory cell array. The memory cell is connected to a plurality of local detection meanses, detecting the information of the memory cell and local detection means. A plurality of scanning amplification meanses amplifying the detection information is included.

84 Moreover, the semiconductor memory is characterized by including a plurality of other memory cells which a plurality of memory arraies is connected to the same word line; and accumulates the reference information which uses when judging the value of the information accumulated in the memory cell for the information and a plurality of memory cell for the information remembering the information.

85 And the semiconductor memory is characterized by including the register means which is adjacent to the memory array and it is arranged; and provisionally accumulates the information accumulated in the memory cell.

86 Moreover, the third semiconductor memory of the present invention is characterized that the memory cell for the information remembering the information, the first bit line, the reference memory cell accumulating the reference information, the second bit line, the first and the second global bitline, the respective first amplified and the second pre-amplifier means the information of the l and the second global bitline, and the sense amplifier are included. As to the first bit line, the memory cell for the information is connected. The reference memory cell accumulating the reference information uses when judging the value of the information accumulated in the memory cell for the information. As to the second bit line, the reference memory cell is connected. As to the first and the second global bitline, the respective first detected and the second number of probe simple fruit, and the detect information of the first and the second probe means are the information of the first and the second bit line delivered. As to the sense amplifier, the output of the first and the second pre-amplifier means is inputted to the input terminal.

87 And provided is the semiconductor memory, in which the first and the second probe means are composed of the MOS transistor having the first conductivity; and the first and the second pre-amplifier means are comprised of the MOS transistor having the second conductivity of the opposite polarity and the first conductivity.

88 Moreover, provided is the semiconductor memory, in which the output of the pre-amplifier means amplifying the information of the reference memory cell is commonly inputted about a plurality of sense amplifiers.

89 The fourth semiconductor memory of the present invention is characterized that the calibration means and the correction sequence compensating for the operation deviation of the sense amplifier are comprised.

90 Provided is the semiconductor memory, in which the calibration means is composed of the condenser

connected to the input terminal of the sense amplifier.

91 The fifth semiconductor memory of the present invention is characterized that the memory cell for the information remembering the information, the first bit line, the reference memory cell accumulating the reference information, the second bit line, the first and the second global bitline, the respective first amplified and the second pre-amplifier means the information of the first and the second global bitline, one end in the output end of the first and the second pre-amplifier means is the respective connected first and the second condenser means, and the sense amplifier are included. As to the first bit line, the memory cell for the information is connected. The reference memory cell accumulating the reference information uses when judging the value of the information accumulated in the memory cell for the information. As to the second bit line, the reference memory cell is connected. As to the first and the second global bitline, the respective first detected and the second number of probe simple fruit, and the detect information of the first and the second probe means are the information of the first and the second bit line delivered. As to the sense amplifier, the input terminal is connected to the other end of the first and the second condenser means.

92 Moreover, the semiconductor memory is characterized by including the short circuit means short-circuiting the terminal of the sense amp side of the corrected transposition configuration method, setting the corrected transposition to the first and the second bit line and condenser means.

93 The signal transfer system of the present invention is characterized that it shows with a plurality of signal line groups in which the predetermined signal is transmitted and a plurality of reference potential signal late kings, and the capacitive means is included. As to a plurality of reference potential signal late kings, it transmits the signal showing the reference potential as the predetermined signal and the other signal. The capacitive means capacitively connects the interval of a plurality of reference potential signal late kings and plurality of signal line groups.

94 Moreover, provided is the signal transfer system, in which the signal line group and reference potential signal late king are nearly parallelly arranged; and it nearly meets at right angle and the capacitive means is made with the signal line group and reference potential signal late king of the arranged intersection ventral grouped gland.

95 Provided is the fifth semiconductor memory of the present invention and signal transfer system, in which a plurality of signal line groups are comprised of the first global bitline receiving the information of the memory cell for the information remembering the information via the first bit line; and a plurality of reference potential signal late kings is comprised of the second global bitline receiving the reference information of the reference memory cell accumulating the reference information which uses when judging the value of the information accumulated in the memory cell for the information via the second bit line.

96 Moreover, the sixth semiconductor memory of the present invention is characterized that the nonvolatile information is maintained since the memory cell is destroyed.

97 Provided is the semiconductor memory, in which the break down of the memory cell consisting of the capacity and transistor is performed with the break down of the heredity thin film forming the capacity.

98 Moreover, the seventh semiconductor memory of the present invention is characterized that a plurality of redundancy information storage cell groups memorizing the redundancy information is included. The information which determines whether the storage cell group of the magnetism is a valid or not whether it is an invalidation or not is included in each redundancy information storage cell group.

99 And the eighth semiconductor memory of the present invention is characterized that the information of the designated value is written in the information storage cell. The information is read after the progress of the designated time. The value of the information written as described above and break down of the other inforamtion are detected and the value of the information read as described above performs the read of the nonvolatile information memorized in the information storage cell in advance.

100 Moreover, provided is the semiconductor memory, in which the designated time to the read of the information from the inscribe of the information is 0.01 millisec or 10 millisec.

101 And provided is the semiconductor memory, in which the nonvolatile information memorized in the information storage cell in advance is the redundancy information; it reads within the predetermined time since inputting power the redundancy information; and the strong with the wave redundancy information is set up as the redundancy circuit.

102 Moreover, the ninth semiconductor memory of the present invention is characterized that it has the redundancy circuit having the variable coding region canning be programmed.

103 And the tenth semiconductor memory of the present invention is characterized that the redundancy information storage cell group having the memory cell of the complementary dehiscence memorizing the redundancy information, the write means, the transmission method transmitting the redundancy information read with the readout means with the redundancy decoder, and the decode means are included with the break down of the heredity thin film. The write means writes the redundancy information in the redundancy information storage cell group it has the other memory cell which remembers the information it is an invalidation the cell group of the magnetism is a valid on the redundancy information storage cell group and the readout means making out the redundancy information. The decode means can change the coding by using the redundancy information transmitted with the transmission method.

104 Moreover, provided is the semiconductor memory, in which the redundancy information memorized in the redundancy information storage cell group is the redundancy information after being compacted; the redundancy information read with the readout means the decompression processing of the redundancy information is performed; and it is transmitted with the transmission method to the redundancy decoder.

105 And the eleventh semiconductor memory of the present invention is characterized that the redundancy information storage device, the readout means reading the redundancy information stored in the redundancy information storage device, the decompression processing means extending the redundancy information read with the readout means, and the transmission method transmitting the redundancy information extended with the extension treatment means with the redundancy decode means are included. As to the redundancy information storage device, the compacted redundancy information is stored.

106 Moreover, the first semiconductor IC of the present invention is characterized that the logic circuit block changing the circuit configuration, the circuit configuration information storage means, the internal information storage means, and the control means are included. The circuit configuration information storage means the circuit configuration information of the logic circuit block is stored. The internal information storage means the internal information of the logic circuit block is stored. The control means while changes the configuration of the logic circuit block based on the circuit configuration information stored in the circuit configuration information storage means, performs data processing based on the internal information stored in the internal information storage means at least as the whole.

107 And the semiconductor IC is characterized by including the common register performing the transfer of the information between 2 logic circuit blocks.

108 Moreover, provided is the semiconductor IC, in which the logic circuit block is fully equipped plural number; and the transfer timing of the circuit configuration information stored in the circuit configuration information storage means crosses each other in a plurality of logic circuit blocks.

109 And the second semiconductor IC of the present invention is characterized that a plurality of unit logics changing a function, a plurality of wiring channels intersecting with an plurality of input-output lead-out wirings extended from a plurality of unit logics, the switching circuit, and the control means memorizing the connection information of the wiring by the switching circuit and channel with plural species, and selects as the memory information of the middle one and controls the switching circuit is included. The switching circuit selectively electrically connects a plurality of input-output lead-out wirings and plurality of wiring channels.

110 Moreover, the third semiconductor IC of the present invention is characterized that the condenser, in which a source and drain are 2 wirings connected to 2 wirings between the respective connected *** MOSFET, and the gate and fixed electric potential of *** MOSFET MOSFET for the load in which the gate of *** MOSFET and load wiring and source and drain are connected, and a source is connected to the gate of MOSFET for the load. It has MOSFET for the CELP boot in which a drain is connected to the load start signal line. The gate of MOSFET for the CELP boot is connected to the other fixed electric potential.

111 And provided is the semiconductor IC, in which the switching circuit is made of *** switch going with 2 wirings; and the signal level of 1 of the power voltage level of the unit logic and load wiring are nearly low set up as the threshold voltage of *** MOSFET.

112 And the first semiconductor memory having data handling function of the present invention is characterized that the first area, the second part, and data processing block reading a plurality of datas of the first area, and collects these datas and processes, and writes the process result in the second part is included. As to the first area, a plurality of datas is stored. The second part is possible to store data.

113 Moreover, the second semiconductor memory having data handling function of the present invention is characterized that the first memory array having a plurality of memory cells connected to a plurality of word

lines, the second memory array having a plurality of memory cells connected to a plurality of word lines, and data processing block is included. The data processing block makes out data memorized in the memory cell connected to the word line of the fixed number from the first memory array, and it collects these datas and it processes, and writes the process result in the memory cell connected to the word line of the fixed number of the second memory array.

114 And provided is the first having data handling function of the present invention, and the second semiconductor memory, in which data processing block compresses data read.

115 And provided is the first having data handling function of the present invention, and the second semiconductor memory, in which data processing block extension-processes data read.

116 Moreover, the third semiconductor memory having data handling function of the present invention is characterized that dynamic, 1 or a plurality of data processing blocks changing a configuration, the first memory cell group, the second memory cell group storing data group to be connected to the second word late king and have to process, and the third memory cell group is included. The data processing block reads data group processed as described above and processing specification information. And data group to process as described above is processed based on the treatment means information. The process result is stored to the third memory cell group. The first memory cell group is connected to the first word line group and data processing specification information of data processing block is stored. The third memory cell group is connected to the third word late king and stores the process result.

117 And the third semiconductor memory having data handling function of the present invention is characterized by including data processing block is the reprogrammable reconfiguration logic.

118 Using the configuration described in the above, since it fits to the electric potential degradation caused by the leakage current of the signal charge in which the electric potential of the information corresponding to the memory cell for the information storage and the reference potential memorized in the other memory cell is remembered in the memory cell for the information storage in the present invention and the electric potential is degraded, the time to the time in which the number of the electric potential difference between both sides reaches the sense limit is extended and data retention time is lengthened.

119 The above-described purpose, the miscellaneous purpose, the characteristic of the present invention and advantage are evident than the detailed description relating with the attached view.

120 (the example in the thread)

121 (the first preferred embodiment)

122 Referring to Fig. 1, below, and the embodiment of the present invention decide to be illustrated.

123 As to (a) of Fig. 1, 11~15 is a plurality of memory cells (the memory cell for the information) remembering the information. These cells belong to the first memory cell group (50). 2 is the memory cell (the other memory cell) belonging to the second memory cell group (51). As to WL, as the word line, a plurality of memory cells (11~15, 2) of the first and second memory cell groups (50, 51) is commonly connected about the same word line (WL). And memory cells (11~15, 2) abbreviated in (a) of Fig. 1 are made of concretely, (b) of Fig. 1 a , circumstantially, as shown in the figure, the cell transistor (Tr), and the cell coverage (C). And in Fig. 1, the word line (WL) 1 shows. But it in fact exists plural number. It is connected to the word line in which the different cell belonging to the l memory cell group (50) according to each word line and the different cell belonging to the second memory cell group (51) are identical.

124 The cell belonging to the first memory cell group (50) is connected to the differential input terminal of the sense amplifier (SA1~SA5) corresponding to through the respective bit line (bit1~bit5). Similarly the cell (2) of the second memory cell group (51) is connected to the readout circuit (53) through the bit line (bit7). In the cell (2) of the second memory cell group (51), the suitable electric charge is nearly accumulated in a median of the electric charge corresponding to the information, corresponding to the reference potential for example, "1" information and the electric charge corresponding to "0" information. The readout circuit (53) makes out data of the cell (2). Read data is commonly inputted to the other differential input terminal of each sense amplifier (SA1~SA5).

125 The sense amplifier (SA1~SA5) makes out the information accumulated in the cell (11~15) comparing the information from one cell (11~15) corresponding with the information from the cell (2) and corresponds to.

126 (the changed example of the first preferred embodiment)

127 The changed example of the first preferred embodiment is shown in Fig. 2.

128 The upper point of this changed example and the first preferred embodiment is the second memory cell group (51) include 2 memory cells (2, 3). In one memory cell (2), the suitable electric charge is accumulated in "0" information. The suitable electric charge is accumulated in the memory cell (3) on the other side in "1" information. The information of 2 theses are transmited through the respective bit lines (bit7, bit8) in the intermediate value generation circuit (the reference potential generating circuit) (54). The intermediate value generation circuit (54) is transformed to the reference potential which is the intermediate potential and the reference potential is transmited to each sense amplifier (SA1~SA6). It determines "1" or "0" of data included in the memory cell in which these sense amplifiers correspond.

129 And as to the first preferred embodiment and changed example, the information accumulated in a plurality of memory cells is not limited to 2 value of "0" and "1". Is a plurality of states ***. What has with an aliquot what is what is called, the pluridentate memory.

130 Next, as to the first preferred embodiment and changed example, it decides to illustrate with the configuration described in the above based on Fig. 3 to draw data retention time. In Fig. 3, the upper shows the time variation of electric potential (the electric potential of the storage node memorizing Vw1, and "0" information the electric potential of the storage node remembering "1" information is expressed in Vw0) of the storage node of the memory cell at the conventional configuration. The bottom side shows the variations of interconnections of the storage node of the storage node of the cell belonging to the first memory cell group at the present invention and the cell (the reference cell) belonging to the second memory cell group. As shown in Fig. 3, the enlargement of data retention time can be achieved.

131 And the reference cell (2) exists according to each word line. Therefore, the time till being read from the point of time when data are entered is different according to the word line. And yet, the time to the time read from the point of time when data are entered is completely agreed between the information cell (11~16) and reference cell (2). Therefore, the exact operation is guaranteed.

132 (the second preferred embodiment)

133 Figs. 4 and Figs. 4 shows the second preferred embodiment of the present invention.

134 Fig. 4 is a schematic configuration diagram of the whole. Fig. 5 is a detail view of each element.

135 In the present preferred embodiment, the above-described first memory cell group (50) is classified into 2 top and bottoms among the drawing and the second memory cell group (51) is arranged in the center area of the interval. As to the batch configuration, the first and second memory cell groups (50, 51) receive the same noises on the whole, and it aims at the effect of the noises solution that the transmission of the reference information of the first memory cell group (50) is performed in the time to be well the same with symmetric from the second memory cell group (51) accumulating the reference information.

136 And particularly the case in which the number of cell connected to the word line which is identical in Fig. 4 in the second memory cell group (51) is 1 is shown. But the configuration of Fig. 2 is employed. In this case, it is necessary to have the median formation circuit (54) of Fig. 2.

137 As to Fig. 4, 55a~55d is the memory array. It has the word line (WL) of the respective plurality of, and the memory cell (MC, 2) belonging to the bit line (bit) and the first and second memory cell groups (50, 51). PRB1, and PRB2 are the plurality of local probes (the local detection means) corresponding to the respective memory array and is arranged. The number is the number like a plurality of bit lines (bit) belonging to the memory array (55a~55d) corresponding to. It functions as the signal detection circuit which is connected to the respective bit line (bit) corresponding to and detects the data. The output of each local probe (PRB1, PRB2) is inputted to one side differential input terminal of the sense amplifier (the scanning amplification means) (SA) through the respective global bitline (Gbit) corresponding to. In each global bitline (Gbit), although not illustrated, it is used in common between the local probe (PRB1,PRB2) positioned in the same column. Therefore, it makes the capacity of the wiring connected to the sense amplifier (SA) small as much as the global bitline (Gbit) is used in common.

138 Data of the memory cell (2) maintaining the reference signal level is assimilated to the readout circuit (53) to the likeness via the local probe (PRB). The output of the readout circuit (53) is delivered to the other side differential input terminal of a plurality of sense amplifiers (SA). The output of each sense amplifier (SA) is accumulated in the SRAM register (the register means) (56) corresponding to. one is selectively drawn out by the column decoder (57) among these outputs. The output of each sense amplifier (SA) is amplified with the output

amplifier (58) and it is outputted to the other circuit block or the outside of chip. In the read operation, the SRAM register (56) is essentially unnecessary. But when excluding the time data read and re-recording in the memory cell read, it functions as the shelter domain for a while.

139 Next, the detail of Fig. 4 the concrete circuit configuration decides to be illustrated based on Fig. 5.

140 As to the upper of Fig. 5, the bottom side shows the second memory cell group (51) the first memory cell group (50).

141 As to Fig. 5, a plurality of memory cells (it says to be below, and the information cell lice) (MC) accumulating the memory information in the first memory cell group (50) is equipped. These information cell (MC) 64 is connected to one word line (WL) to the low direction. Is a parallel. The information cell (MC) positioned in the same column of a plurality of (2 in the drawing) is connected to the bit line (the first bit line) (bit1). The bit line (bit1) is connected to the global bitline (the first global bitline) (Gbit1) through the local probe (the first probe means) (PRBa). The global bitline (Gbit1) is connected to one side differential input terminal of the sense amplifier (SA) of the latch type via the preamp part (60).

142 Similarly, in the second memory cell group (51), a plurality of memory cells (it says to be below, and the reference cell lice) (2) accumulating the reference information is equipped and each reference cell (2) is connected about the word line (WL) of the respective 1. The reference cell (2) positioned in the same column of a plurality of (2 in the drawing) is connected to the bit line (second bit line) (bit2). And the bit line (bit2) is connected to the global bitline (second global bitline) (Gbit2) through the local probe (the second probe means) (PRBb). The global bitline (Gbit2) is commonly connected to the other side differential input terminal of a plurality of sense amplifiers (SA) via the preamp part (61). In each sense amplifier (SA), the output of the global bitline (Gbit2) is inputted to the gate of the built in input transistor (N17) via the preamp part (61). Therefore, it does not have an effect on the operation of the sense amplifier (SA) even if the wiring capacitance of the global bitline (Gbit2) is enlarged.

143 Next, the detailed construction decides to be illustrated with the operation of the whole. Fig. 6 shows Fig. 7 is the state of the major control transistor at the content (mode) of each control the operating waveform is shown. The content of each control is as follows.

144 (precharge period)

145 Bit lines (bit1, bit2) are pre-charged till the voltage (Vdd-Vtn) degraded with the NMOS control transistor (N11, N21) from the power supply voltage (Vdd) as the threshold voltage (Vtn). In the meantime, the global bitline (Gbit1, Gbit2) is pre-charged in the voltage (Vss+Vtp) which is higher than the ground voltage as the threshold voltage (Vtp). And the precharge level described in the above essentially does not change as to the other value, for example, the ground voltage (Vss). Similarly, as to 2 differential input terminal node (Nsig, Nref), a pair of the node (NsenA, NsenB) of the sense amplifier (SA) is altogether set up as the power supply voltage (Vdd) as the ground voltage (Vss).

146 (cell reader)

147 The word line (WL) is activated and reference information data in which memory data accumulated in the information cell (MC) of the first memory cell group (50) are accumulated in the bit line (bit1) in the reference cell (2) of the second memory cell group (51) is read in the bit line (bit2). Therefore, according to the electric potential of the bit line (bitl) is "1" of memory data or "0", as shown in Fig. 6, it is changed. At the same time, the transition of the bit line (bit2) is changed in the reference potential as the suitable electric potential.

148 (the read of the global bitline)

149 The electric potential of each global bitline (Gbit1, Gbit2) is changed according to the electric potential of bit lines (bit1, bit2) in which the read control transistor (N13, N23) of each local probe (PRBa, PRBb) attains enlightenment and corresponding to. Therefore, the respective accumulated memory information and reference information are read in the information cell (MC) and reference cell (2) in the respective global bitline (Gbit1, Gbit2).

150 (pre-amplifier read)

151 The reference potential information and the memory information in which PMOS type transistors (p13, p23) of each preamp part (60, 6l) attain enlightenment and which is read are inputted to the sense amplifier (SA) through the node (NSig,Nref). It is available with the determination of data. And in the present preferred embodiment, as to the reason for arranging preamp parts (60, 61), in the reference information input side of

the sense amplifier (SA) is a plurality of sense amplifiers (SA), the load of the input side is due to be enlarged as the common.

152 (sense operation)

153 The memory information is sensed with the sense amplifier (SA). The sensed memory information is maintained in the inside latch.

154 (the rewrite of data)

155 Using the rewrite circuit (RST1), and, at the same time, the reference date of accumulated knowledge data is filled in the information cell of the first memory cell group (50) with the standards write circuit (STR) in the reference cell (2) of the second memory cell group (51).

156 (the third preferred embodiment)

157 Next, the third preferred embodiment decides to be illustrated based on figs. 8 and figs. 8 This embodiment is the reorganization embodiment of the second preferred embodiment.

158 As to the embodiment described in the above, the object of this embodiment has to avoid the phenomenon that the substantial input voltage of the sense amplifier (SA) is reduced due to the deviation of the signal transfer characteristic between 2 preamp parts (60, 61) between 2 local probe (PRBa, PRBb). That is, it makes a deviation, the lot, and the actuating margin small as the amount of the sum of the difference of the critical value (Vtp) of the control transistor (P14, P24) of 2 preamp parts (60, 61) of 2 local probes. In the present preferred embodiment, a deviation is avoided by utilizing the condenser for a correction.

159 The procedure of a correction is as follows.

160 As to Fig. 9, the transistor switch (CL1) and the other transistor switch (short circuit means) (CL2) attain enlightenment and each global bitline (Gbit1, Gbit2) of the standards dragon and information is charged with the fixed voltage (V_{CALA}). Simultaneously, the input voltage of the sense amplifier (SA) is charged with the other fixed voltage (V_{CALB}). At this time, the bit line entry switch (CW) attains enlightenment. The fixed voltage (V_{CALA}) is filled in each bit line (bit1, bit2).

161 Next, the entry switch (CW) is not connected. The transistor switch (GPR) attains enlightenment and each global bitline (Gbit1, Gbit2) of the standards dragon and information is together charged with the low level (the Vss or Vss+Vt). Thereafter, the control transistor (N12, N22) of each local probe (PRBa, PRBb) is activated. Therefore, the electric potential of each global bitline (Gbit1, Gbit2) of the information and standards dragon rise than the electric potential of bit lines (bit1, bit2) corresponding to as the threshold voltage (Vt) to the low electric potential. At this time, in the electric potential of each global bitline of the information and reference axis, the electric potential difference corresponding to the difference of the threshold voltage (Vtn(data), Vtn(ref)) of the NMOS control transistor (N12, N22) of the information and reference axis exists.

162 And then, control transistors (p13, p23) of each preamp part (60, 61) of the information and reference axis are activated. The electric potential of each global bitline (Gbit, Gbit2) is read among the drawing of condenser (the first and the second condenser means and calibration means) (Ccal1, Cca12) for the respective first and the second correction to the left end. V_{CALA} - Vtn (data) -Vtp in the information the value of the electric potential does the Vtp (data), and the threshold voltage of the PMOS type control transistor (p23) of the reference axis about the threshold voltage of the PMOS type control transistor (p13) of the information to the Vtp (ref) (data)

164 In the reference axis it becomes.

165 It consists of V_{CLAA} - Vtn (ref) - Vtp (ref) (and, the Vtp (data), and the Vtp (Ref) <0).

166 - [Vtn(data) -Vtn(ref)] - [Vtp(data) -Vtp(ref)] due to the deviation of the threshold voltage of the information and reference axis 2 values originally completely coincide with.

168 It is generated to go miss with ***. This lowers the actuating margin of the whole. A difference is memorized in the condenser (Ccal1, Cca12) for a correction. Therefore, because of a deviation being absorbed and compensating and expecting the actuating margin of the sense amplifier (SA), it can secure with a large.

169 The effect of a correction is shown in Fig. 10. In case (a) of Fig. 10 does not have a correction, it shows the

case where the case has (b) of Fig. 10 . As shown in it can know from Fig. 10, the deviation of the signal voltage in the input terminal of the sense amplifier (SA) is reduced. The stabilized operation can be realized.

170 The correction sequence is comprised of the operational sequence described in the above. And the correction electric potential establishment means is comprised of the transistor switch (CL1) and bit line entry switch (CW).

171 And figure 8 shows the configuration of the case of mixing the memory (DRAM) and logic circuit on one chip. (a) of Fig. 8 has the configuration listing the sub block (60) consisting of the pre-amplifier of Fig. 9 and sense amp area (A), and part (B) with a plurality of (8 in the drawing 10). Sub-word drives (61, 62) selecting the respective word line are arranged in the upside or the downside of a plurality of sub blocks (60). A pre-amplifier and sense amp area (A) are arranged in the right among the drawing of the sub block (60) of the among drawing dexter edge end. As to (a) of Fig. 10, the block (63) consisting of the configuration of (b) of Fig. 10 is arranged in a lenghtwise with a plurality of (M). Simultaneously, the logic circuit (64) is arranged in the among drawing right. Therefore, the simultaneous transmission of multi-bit data of the logic circuit (64) is possible from the register circuit (65) of the sense amp area (A) and the pre-amplifier which the bundle-branch block (60) has.

172 (the fourth preferred embodiment)

173 And then, the fourth preferred embodiment of the present invention decides to be illustrated. This embodiment more and more reduces the noises in an operation and it enlarges the actuating margin. In the present preferred embodiment, the noise factor which is called because of being what is called, the array noises is minimally done.

174 As to the array noises, the node, expanded in the memory array whole and read signal line capacitive-couple. Consequently the read signal line ceremony change refers to the noises which again returns to the read signal line. Data which are called because of being an ordinarily, and the fraction bit therefore cause the reader error the noises.

175 As to (a) of Fig. 11, for example, data of "1" is read in the global bitline (i) for the information. The case where data of "0" is read in 1, 2, I-1, I+1렁?of the except can be considered. In this case, the memory array whole is taken to the direction making out data of "0" for the bit line interval or the plate with the capacitive coupling. Consequently, data of "1" read from the global bitline (i) for the information materially reduces. The false reading is therefore generated.

176 In the present preferred embodiment, the false reading described in the above is solved with the following configuration. That is, arranged so that the floating wiring (capacitive means) (M1) span on both sides of each global bitline (1? i?, R) of the information and standards dragon. Here, the floating wiring (intersection ventral grouped gland) (M1) is the effectivelyelectrically wealthy wiring according to the name. Even in case of being connected through the high value resistor to the fixed electric potential, it can regard as the similarlyeffectively wealthy wiring.

177 The feature point of this embodiment is the point in which the wiring (M1) is arranged in order to extend into both sides of each global bitline (1? i?, R) of the information and standards dragon. The information dragon within an array and standards suspicion global bitline (1? i?, R) unites through the floating wiring (M1). The potential variation divides the direction of the read data evenly. The mean value again unites with the global bitline (R) for the standards through the capacitive coupling. If there is countless "1" data among read data, the electric potential of the floating wiring (M1) changes to the direction making out "1" data. Thus, it fits and it changes to the it is similar direction. It can be therefore increased the signal margin of the decimal "0" data reading line.

178 For example,, in case it does not have the capacitive coupling of the global bitline (R) for the standards, it has no concern with the global bitline (R) for the standards, it moves only "0" data reading line. The read of "0" data accurately does not perform. It can change if the number of intensity of the inter-combined within the memory array is the floating wirings (M1) is changed. The signal level therefore can control to the most suitable state.

179 In (b) of Fig. 11, the noise reduction effect of this embodiment is shown. As to (b) of Fig. 11, the horizontal axis is the parameter defined as data isolation coefficient (Data Isolation Ratio) (R0). When being R0=1, data on the identical word line altogether shows as "0" data to be occupied. It altogether shows R0=0 days the case to be "1" data. The longitudinal axis is the signal electric potential at the sense amplifier input terminal. The sense limit is exceeded in data read of "1" and a signal is outputted. In the present preferred embodiment, it is possible that as shown in it can know from (b) of Fig. 11, it exacts, decoding-operate through the entire region of the correction data isolatation coefficient (RO) of this embodiment.

180 In Fig. 12, data retention characteristic of DRAM is shown. It is possible that as shown in it can know from Fig. 12, in the present preferred embodiment, data retention characteristic is improved with the White heat digit.

181 (the fifth preferred embodiment)

182 Next, the fifth preferred embodiment of the present invention decides to be illustrated. This embodiment is the configuration of the redundancy method which this embodiment uses in the DRAM of the present invention.

183 Generally the redundancy method is used for DRAM. It refers to the circuit substituting for the bad memory cell with the electrically normal memory cell. Generally the redundancy circuit can divide into the redundancy address detection circuit, memorizing the information (the redundancy information) of *** the address and this of the bad cell as any kind of reserved memory (the redundancy address) and the redundancy address circuit converting the address based on the information in fact.

184 The conventional redundancy address detection circuit is shown in (a) of Fig. 13 and the conventional redundancy address circuit is shown in (b) of Fig. 13. In (a) of Fig. 13, it is the media memorizing the redundancy information. The fuse (F) formed owing to the wiring layer including a polysilicon etc. is utilized. This fuse (F) is cut with the laser trimmer apparatus and the redundancy address information is remembered. The cut of a fuse determines as existence and nonexistence of the current path which is an electrical. It transmits the decision result to the redundancy address circuit and existence and nonexistence perform the change over of the actual address.

185 Concretely, firstly, as to (a) of Fig. 13, the scanning node (Knr) is precharged to the power supply voltage (Vcc) level by using the pre-charge transistor (70). Next, if the address signal line (Ai, xAi, Aj, xAj) is changed, the scanning node (Knr) is not discharged about the address in which a laser cuts the fuse (F). In (a) of Fig. 13, the scanning node (Knr) is not discharged only when being Ai=1, and Aj=0. The redundancy enable signal (REN) is activated when being the address. The redundancy word line (?R) is activated by the signal (REN). Simultaneously, the regular word line (?WL) is deactivated.

186 It is based Fig. 14 and the redundancy method of this embodiment decides to be illustrated.

187 In the present preferred embodiment, the mode memorized is employed to whether or not of the paper in which the capacitive film within the memory cell of DRAM is the redundancy information destroyed. Here, the capacitive film is formed owing to an ordinarily, the silicon oxide film, the silicon nitride film, the sandwich structure, or the tantal oxide layer, including, the high dielectric layer etc. The information is stored with the break down of these films, and a non-destructive.

188 At the same time, the inscribe of the redundancy information of the capacitive film of the memory cell is performed in the probe inspection based on the following order.

189 Firstly, the redundancy information storage cell includes. All memory cells are inspected. It measures. At this time, in case the redundancy information storage cell breaks down, a series of redundancy cell including the malfunction cell is not used. The other series of redundancy cell is used. And at the same time, invalidity flag data showing a two-phase is written in the flag area of the redundancy cell voided as described above with the other redundancy information. The inscribe of this information sets the suitable electric potential at the bit line connected to the redundancy memory cell ruined at "0". The inscribe of this information performs by high setting up the plate voltage than the external power supply. In the redundancy memory cell which is not destroyed, the plate voltage is set up as the power supply voltage or the floating level. And as to (a) of Fig. 14, 72 is data scanning system having the register (65) a configuration among the configuration of Fig. 9. And as shown in the white circle among (a) of Fig. 14 is (b) of Fig. 14, the memory cell in which the capacitive film is not destroyed is exemplified. The black circle exemplifies the destroyed memory cell.

190 Next, the method for making out the information filled in the redundancy cell with the break down inscribe of the capacitive film decides to be explained.

191 Firstly, data of "0" is written in the whole of the memory cell including the redundancy information. At this time, the plate voltage is set up as the power supply voltage. In the redundancy cell in which head and face, and the capacitive film are the time of 0 Olms. or about 10ms destroyed after an inscribe, stored data are applied in the plate voltage and data invert into "1". In the dissimilar side, and the cell of a non-destructive, data of "0" is maintained. Data is read as the redundancy information. After the redundancy information is stored in the register (73), it serially transmits with the redundancy circuit (the mention later) at high speed by using the serial transfer circuit (the transmission method) (74).

192 The leaving alone time (0.01~10ms) after an inscribe is the time or greater till all electric charges are nearly

emitted from the destroyed capacitive film. It is enough long than the normal read time of data. It is the time to be enough short than moreover, the normal data retention time. In case the redundancy cell group is an invalidation and the flag is detected, the electrical transmission of the information skips. A detection and control of the redundancy address are performed based on the or more. The electrical transmission of redundancy data automatically performs in the power up. The next operates only the redundancy circuit. And "1" is written in the memory cell. It is *** to accomplish the purpose of being the same as to the method for setting up the plate as "0".

193 The configuration of the redundancy circuit (71) canning be programmed is shown in Fig. 15. It has 2 coding regions. The redundancy information is serially transmitted to the variable coding region (75) in the power up from the serial transfer circuit (74) of Fig. 14.

194 In the variable coding region (75), a plurality of programmable switch elements (PS1~PS8) is equipped. The redundancy information is serially transmitted in these according to the order of number from the serial transfer circuit (74). In order to be generated the redundancy enable signal (REN) from the variable coding region (75) when being the malfunction address according to the redundancy information these are comprised. The conduction (the black coating display), and the other device of 15 switch element (PS4, PS8) exemplifies a thing generated around the address signal Ai=1, and the redundancy enable signal (REN) in a xAj=1 days it does. The redundancy enable signal (REN) is outputted to the canonical decode inhibit circuit (77) and it suppresses the electrical transmission of the canonical decode signal (?wl~?w4) from the fixing coding region (76).

195 And in the present preferred embodiment, it divided into the variable coding region (75), and fixing coding region (76). But the whole is to the variable coding region. In this case, the canonical decode inhibit circuit (77) is unnecessary. The high speed is attempted as that. But the coding area is on the increase.

196 The redundancy detection is performed among in the inside of the normal static circuit in case of using the circuit configuration described in the above. Consequently the redundancy system in which the working speed is fast can be realized with the low current consumption. And according to a part of the external address the electrical transmission of the variable decoding domain (75) of the redundancy information, it remarkably makes the circuit size of the redundancy circuit (74) small if it appropriately performs. The reduction of the chip area can be realized.

197 And the redundancy information memorized in the redundancy cell group of Fig. 13 is compressed and it memorizes in the redundancy cell group. If the decompression processing is performed in the read of the information and the read transmits in the redundancy circuit, the number of the redundancy cell group can be cut down. The enlargement of the chip area can be held back. As to the conventional fuse redundancy method, the employment of the compression mode of the redundancy information is the mode which is effective in the point cutting the fuse number.

198 And in the present preferred embodiment, as to the redundancy method of DRAM, the present invention was applied to the memory of the redundancy information. But it can apply besides the redundancy. For example, it is possible that the manufacture information of the maker specificinformation, the Holotrichia years, a lot, the chip coordinate etc is accumulated, or and, the analog circuit of an inside, for example, the level calibration information including the internal power supply circuit or the power source level detecting circuit etc. is remembered. It reads in the actual operation and it uses. And the information for most appropriately operating the internal timing generation circuit is remembered. If the information is loaded in a start-up in the timing generation circuit, the semiconductor IC in which the timing margin is more more and more big can be realized.

199 (the sixth preferred embodiment)

200 In the fifth preferred embodiment, the information is memorized with the break down of the capacitive film of the memory cell, and a non-destructive. Therefore, the very big bit width, for example, the memory core of 256~2048 bit width can be formed. Therefore the transfer of data and logic circuit can be performed by using a plurality of data buses. This embodiment is one application example taking advantage of a characteristic.

201 (a) of Fig. 16 tranversely arranges the register group (81) of the memory core (80) of the present invention. It shows the configuration of performing the transfer of data this and logic circuit (82) into a plurality of data buses (83).

202 As the logic circuit (logic circuit block) (82), (b) of Fig. 16 uses the circuit which on the whole, progresses the predetermined processing while appropriately changing the configuration of the logic in the dynamic configurable logic, that is, the operation halfway. 16 memory core (the circuit configuration information storage means, and the internal information storage means and control means) (80a, 80b), 2 register groups (81a,

81b), and the case of performing the transfer of data 2 dynamic configurable logics (85a, 85b) between 2 logics (85a, 85b) through the general purpose register (the common register) (86) are shown. It is performed to the change silver alternation (an interleave) of the logical organization. And the present invention does not limit the memory core artificial arm to 2.

203 Hereinafter dynamic configurable logics (85a, 85b) show the embodiment of the internal configuration of one configurable logic (85a) in Fig. 17 the same composition.

204 Fig. 17 includes the dynamic configurable logic (85a) is a plurality of unit logics (90), and channel wire portion (channel wiring) (91), and a plurality of programmable switch elements (switching circuit) (92) shown by the drawing 15th day of the seventh lunar month. The unit logic (90) refers to the simple AND gate or the function block having the some function. The channel wire portion (91) has a plurality of channel wirings intersecting with an plurality of outgoing lines (93) extended from a plurality of unit logics (90).

205 Each programmable switch element (92) is posted at the intersection point of each channel wiring of each outgoing line (93) and channel wire portion (91). It is converted to the state of the non-conducting shown by the among drawing white circle and the conduction state shown in the black with among drawing circle and it dynamically changes the connection which is the electrical of the channel wiring and outgoing line (93), and the connectionless according to the connection information memorized in the memory core (control means) (80a). It connects a plurality of unit logic (90) intervals and it realizes the actual circuit.

206 In the present preferred embodiment, as shown in (b) of Fig. 17, as shown in (c) of the dynamic switch element utilizing a condenser or Fig. 17, the programmable switch element (92) uses one among the static using the SRAM cell. As the NMOS (*** switch) of *** going with 2 start the deliberation of the bill introduced wiring a source and drain are connected to 17 wiring (x, y), the condenser (c) is arranged between the gate and ground (the fixed electric potential). And as to load, the switch data line (the load wiring) from the memory core , and Load-en is the load enable line (the load start signal line) which designates to load data in *** MOSFET (92a). In the gate and switch data line (Load) of *** MOSFET (92a), the MOSFET (92b) for the load in which (in that is, the gate and switch data line of *** MOSFET (92a)) source and drain are connected is arranged in these. And in the gate of the MOSFET (92b) for the load, the source of the MOSFET (92c) for the CELP boot is connected. As to the MOSFET (92c) for the CELP boot, the drain is connected to the load enable line (Load-en). The gate is connected to the fixed power (the other fixed electric potential).

207 As to (b) of Fig. 17, if the switch element (92a) is passed through "1" level of a signal, it is degraded as the threshold voltage (Vt). Thus, the power supply voltage within the angular unit logic (90) uses the low power than the external power voltage (Vcc) as the threshold voltage (Vt) in order to suppress the penetrating current within the caused unit logic (90).

208 It sums up from the register group (81a) to each switch element (92) and as shown in the connection information which in case it uses the programmable switch element (92) of a configuration, it stores in the switch element (92). Is (a) of Fig. 17, it is transmitted. The connection information is different according to the word line within the memory core.

209 Now, it says to be for convenience, and the connection information of the word line the sheet. As an image, it divides the assembly of the some logic into the sheet. The operation of the total logic is realized while processing these sheets. Here, as to the connection information fixed at each sheet, as used in the above-described redundancy method, it is maintained by the break down of the memory cell, and data write by a non-destructive. And the function of having the angular unit logic (90) is established with the information from the register group (81a). And it dynamics, the logical value of the node within each sheet is stored in the memory core (80a). It is read in the unit logic (90). The memory core (80a) is used even if it is done by the storage location in the operation of the angular unit logic (90) of necessary data for a while.

210 It decides to illustrate for one application example of dynamic configurable logics (85a, 85b) of this embodiment. The application example simplifies a description. A description is very complicated in fact.

211 It can think to realize the processing system performing the following processing.

212 1) The input data A, and B are inputted.

213 2) It is done by the A>B rear side, C?A?B, and D?A?B.

214 3) It is done by the A?B rear side, C?0, and D?1.

215 4) It is done by the A<B rear side, C?B*A, and D?B?A.

216 5) The value C obtained in a processing, and the sum total of D are reckoned and it does to the final output E.

217 As shown in Fig. 18, it becomes if the processing described in the above is described as data flow to a schematically.

218 In case this processing is practiced in the configuration of Fig. 16, it becomes same with a next.

219 The flow of an operation decides to be illustrated by using Fig. 18.

220 Firstly, the connection information of the great small judgement circuit (sheet 1) accumulated within the memory core (80) is loaded in the configurable logic (85a). Next, a, and the great small of B are determined by the logic (85a). one is loaded according to the decision result among sheets (2, 3, 4) in the configurable logic (85a). At this time, first of all, data A, and B are pushed to the general purpose register (86) of (b) of Fig. 16.

221 And then, one processing is performed among sheets (2, 3, 4). The return value C, and D are again stored as the general purpose register (86). Next, the circuit information of the sheet (5) is loaded in the configurable logic (85a). The value (C, D) is processed and E is finally outputted.

222 In this way, in the present preferred embodiment, the circuit size existing in fact can realize the circuit of the sheet 5 field in spite of being the sheet 1 field only. In this case, it can realize with very small area in the number of ream of the sheet can use is the word line of the memory cores (80) since being considerable. The semiconductor of the high-integration ?high function can be with low cost realized.

223 (the seventh preferred embodiment)

224 Next, the seventh preferred embodiment of the present invention decides to be illustrated.

225 This embodiment shows the realization method of the condenser within the memory core and switch.

226 Fig. 19 is a cross-sectional view of the memory cell of this embodiment. Fig. 20 is a cross-sectional view of the conventional memory cell.

227 As shown in Fig. 19, the feature of this embodiment draws up the source electrode (S) of a transistor to the top layer of the wiring after the bit line (100) positioned at the upside, and the global bitline (101). Here it forms the storage node (102). And it forms the dielectric film (103) on and, the storage node (102). It is the point which thereafter forms the plate electrode (104). The plate electrode (104) is made of the conductivity organic film. It is accumulated in the top layer with a method including the spin coating etc. and a method is comprised. In DRAM etc, the plate electrode (104) shows the action of minimally invading the cracking of the alpha ray consisting of a problem.

228 The shape of the storage node (102) has 2 kinds of the rod shape illustrated in Fig. 19, and tulip flower shape illustrated in Fig. 21. In the rod shape of Fig. 19, after the process of the formation accumulates the membrane electrode assembly consisting of the storage node (102), it cuts the membrane electrode assembly with the rod shape with an etching, it makes and here it sediments the dielectric film (103). The process of the formation forms the plate electrode (104) thereafter consisting of the conductivity organic film. In the meantime, in the tulip shape of Fig. 21, the conductivity organic film which firstly consists of the plate electrode (104) is sedimented on the front side. Here a hole is formed. Thereafter, the storage node electrode (102) is tenuously sedimented on the front side. It etches and the storage node electrode (102) on the tulip shape is formed. Next, the dielectric film (103) is sedimented on the front side of the storage node (102). The plate electrode (104) thereafter consisting of the conductivity organic film is formed. As shown in it can know from figs. 19 and figs. 19 the process of the tulip shape side is complex. However, the more big condensor capacitance can be realized.

229 It is different from the conventional thing in which as shown in Fig. 20, a case of 2 memory cells the wiring layer is positioned in the upside of the storage node (102). All process are very the difficult electrode material advantageous for the plate electrode (104) as to the ferroelectrics memory which it need to use that all process process since forming the memory cell after all processes including the wiring etc. terminate. And when this kind of memory cell is compared with the conventional mode the mode in which a cell is positioned in the bit line of the memory cell and intersection point whole of the word line is adopted to realize, the density of the bit line dies. The impression of a node is due to be facilitated.

230 And a material including the conductive poly mid or the conductive poly ethylene etc. is contained. Can absorb

the alpha ray etc. which consists of a reason including the software error etc. among the conductivity organic film consisting of the plate electrode (104) and obtained the semiconductor memory which has the higher reliability if it does moreover, the film thickness over 3 micron can be realized.

231 (the eighth preferred embodiment)

232 Next, the eighth preferred embodiment of the present invention decides to be illustrated. This embodiment relates to the technology which it uses when setting up the semiconductor IC of the present invention which in the above, it illustrates.

233 This embodiment sets up 64M bit SDRAM which it develops by using the memory core which this embodiment illustrates to a shape and this embodiment is the micro type memory module in the above, it sets up in the motherboard of the personal computer. As to this mode, the package of a semiconductor nearly like that consists of the memory module (DIMM(Dual-In-line Memory Module)).

234 In (a) of Fig. 22 the section structure of the memory module, and the shape of a connector on the motherboard corresponding to a module is shown in (b) of Fig. 22.

235 The x32 SDRAMs (101) is set up by using the MCM technology. The connector shape of 2 heat is realized with this configuration. Using this configuration, the DIMM structure of it being near can be realized with the length and about thickness 3mm of 3cm in 200 pin.

236 This structure can do the wire length of the memory on a motherboard to a minimum. This structure makes data transmission which is the high speed between the logic chip and the memory possible. The dumping resistance corresponding to SSTL is built in inside a connector.

237 As shown in (b) of Fig. 22 it is the small memory module as described above, it can use in both sides of the desk saw PC and note type PC to the same. The low price can be more realized.

238 (the ninth preferred embodiment)

239 Next, the ninth preferred embodiment of the present invention decides to be illustrated.

240 Fig. 25 is a detail view of the internal configuration of the memory (semiconductor memory) having data handling function.

241 As to Fig. 25, first and the second memory array (A, B) having second multi-bit data bus (160) of the respective about 1024 bit are positioned at the left part and right part. Is inserted between the memory array (A, B) and the switching matrix S heat (150?) and programmable logic (PL?) are arranged as the array shape. The data processing block (130) reconstructing a reprogrammable is comprised of the switching matrix S heat (150?) and the programmable logic (PL?) arranged in the central part. And the configuration of the reconfigurable logic does to the configuration of the dynamic reconfigurable logic (85a) illustrated in Fig. 17. The control circuit (170) controls the memory array (A, B), and the switching matrix S heat (150?) and programmable logic (PL?). These are formed within the module of one chip or SIMM or DIMM.

242 As to the first memory array (A), the first memory cell group (151) is connected to the first word line group (149). Simultaneously, data processing specification information of data processing block (130) is stored in a plurality of memory cells. And the second memory cell group (the first area) (153) is connected to the second word late king (152). Simultaneously, data group processed are stored in a plurality of memory cells. And as to the second memory array (B), the third memory cell group (the second part) (155) is connected to the third word late king (154). Simultaneously, a plurality of memory cells is to the place storing the process result.

243 Here, each switching matrix S heat (150) performs the exchange of data of bit liver (upward and downward in the drawing) of the exchange of data with the programmable logic (PL) and the second multi-bit data bus (160).

244 The operation of the memory having below, and data handling function of this embodiment decides to be illustrated.

245 Firstly, the processing specification information of data of the first memory cell group (151) is loaded from one memory array (A) through the second multi-bit data bus (160) in data processing block (130). The processing specification information is made of the connection information of the switching matrix S heat (150?), and the program information of the programmable logic (PL?). The processing specification information is the

information including the compression processing or the decompression processing of the moving picture compressing encoding standard (MPEG2) performed in the DVD device etc. etc. for example.

246 Next, data which is stored in the second memory cell group (153) from the memory array (A) processed is loaded in data processing block (130). The process result at data processing block (130) is stored in the third memory cell group (155) of the memory array (B) on the other side. This a series of operation is controlled with the control circuit (170).

247 And the configuration in which 25 memory array As and B were physically divided was shown. But it does not have the need to be divided.

248 (the 10th preferred embodiment)

249 And then, the 10th preferred embodiment decides to be illustrated. This embodiment again repairs the memory having data handling function shown in Fig. 25.

250 Fig. 26 is a configuration diagram of the memory having data handling function of this embodiment. In Fig. 26, the second multi-bit register (180) is positioned in a center. The data processing block (130', 130') is positioned at the left and right side. Each data processing block (130', 130') is comprised by the switching matrix S heat (150?) and the programmable logic (PL?) arranged as the array shape like the ninth preferred embodiment.

251 Since 2 data processing block (130', 130') can perform the respective operation independantly the necessary time can be covered in the load of the externally data processing specification information. That is, phase 1)

253 One processing unit: data processing, and the processing unit on the other side: the load of the processing method information.

254 Phase 2).

255 One processing unit: the load of the processing specification information, and the processing unit on the other side: data processing.

256 2 phases can be by turns repeated.

257 (the eleventh preferred embodiment)

258 Next, the eleventh preferred embodiment decides to be illustrated.

259 As to this embodiment, by using the memory having data handling function arranging the second multi-bit register (180) to a center like the 10th preferred embodiment, it more more and more makes the use which is a dual-port is the high speed possible.

260 The use which is a dual-port means the configuration of being the same in Fig. 27. That is, the configuration where the memory (MM) having data handling function is used between 2 memory buses (179, 181) as the shared memory is meant. As to Fig. 27, mi , and Mj are the memory of having in other words without data handling function connected to the memory bus (179). Mi , and Mj are controlled with the memory controller (183) within the core logic (182). Similarly, mk, and MI are the memory of having in other words without data handling function connected to the memory bus (181). Mk, and MI are controlled with the memory controller (185) within the core logic (184).

261 The internal configuration of the memory (MM) having data handling function is shown in Fig. 28. As to Fig. 28, the second multi-bit register (180) exists in a center. In order, data processing blocks (130'a, 30'b), and the memory array (A, B) and data I/O parts (186, 187) are positioned at the left and right side to the respective outer side. These are connected to the respective second multi-bit data buses (188, 189).

262 At the same time, the exchange of data at 2 memory bus (A, B) livers and data processing can be realized with this kind of configuration.

▸ Effects of the Invention

263 As described above, according to the present invention, the suitable information is memorized in the memory cell for the information storage and the other memory cell in the reference potential. Even if the electric potential

of the signal charge which is memorized in the memory cell for the information storage since using the information as the reference potential at the sense amplifier is degraded due to the leakage current, the electric potential is extended for the time to the time which the number reaches the sense limit. The excellent semiconductor memory in which data retention time is lengthened and improving data retention characteristic can be realized.

264 The preferred embodiments of the present invention is disclosed for the object of example. And and an addition will be possible through the thought of the present invention and the range disclosed in the patent claim which is attached if it is the person skilled in the art in the world.

Scope of Claims

Claim[1] :

265 The semiconductor memory wherein it is made of the capacity and transistor and the memory cell for the information performing moreover, the read operation of the information, the word line accessing the memory cell, and the memory cell of the other *** and the memory cell connected to the word line having the word line and identity or the same address are included; it is the reference information corresponded to the separate memory cell to the reference potential of the information read from the memory cell for the information; and the information used of the sense amplifier is remembered.

Claim[2] :

269 The semiconductor memory of claim 1, wherein the number of memory cell for the information is more than the number of the other memory cell over 1.

Claim[3] :

271 The semiconductor memory of claim 1, wherein the number of separate memory cells includes the reference potential generating circuit generated around the reference potential based on the information which is accumulated "1" and "0" information in 2 memory cells.

Claim[4] :

274 The semiconductor memory of claim 1, wherein the reference potential generating circuit generated around the reference potential based on the multi-value information which the pluridentate information is memorized in the separate memory cell more than the memory cell for the information more than 3 and 3 are included.

Claim[5] :

277 The semiconductor memory of claim 1, wherein the first memory cell group having the memory cell for the information nearly consists of 2 with the equal cleavage; and the second memory cell group having the separate memory cell memorizing the reference information is arranged in the interval.

Claim[6] :

279 The semiconductor memory comprising: a plurality of local detection meanses, which detects the information of the memory cell it is connected to the memory cell of each memory cell array it includes the memory cell array having the memory cell in which a read and writing operation of the information are possible with plurality it remembers the information and a plurality of scanning amplification meanses which is connected to the local detection means; and amplifies the detection information.

Claim[7] :

282 The semiconductor memory of claim 6, wherein: a plurality of memory arraies include a plurality of memory cell for the informations, and a plurality of other memory cells accumulating the reference information; a plurality of memory cell for the information is connected to the same word line; and remembers the information; and a plurality of other memory cells accumulating the reference information uses when judging the value of the information accumulated in the memory cell for the information.

Claim[8] :

286 The semiconductor memory of claim 6 or 7, wherein it is adjacent to the memory array and it is arranged; and the register means which provisionally accumulates the information accumulated in the memory cell is included.

Claim[9] :

288 The semiconductor memory comprising: the sense amplifier in which the output of the respective first amplified and the second pre-amplifier means and the first and the second pre-amplifier means are the information of the memory cell for the information remembering the information and the first bit line, in which the memory cell for the information is connected and the reference memory cell, accumulating the reference information which uses when judging the value of the information accumulated in the memory cell for the information and the second bit line, in which the reference memory cell is connected and the first and the second global bitline, in which the respective first detected and the second number of probe simple fruit, and the detect information of

the first and the second probe means are the information of the first and the second bit line delivered and I and the second global bitline inputted to the input terminal.

Claim[10] :

296 The semiconductor memory of claim 9, wherein the first and the second probe means are composed of the MOS transistor having the first conductivity; and the first and the second pre-amplifier means are comprised of the MOS transistor having the second conductivity of the opposite polarity and the first conductivity.

Claim[11] :

299 The semiconductor memory of claim 9, wherein the output of the pre-amplifier means amplifying the information of the reference memory cell is commonly inputted about a plurality of sense amplifiers.

Claim[12] :

301 The semiconductor memory, wherein the calibration means the calibration means and the correction sequence compensating for the operation deviation of the sense amplifier are comprised is composed of the condenser connected to the input terminal of the sense amplifier.

Claim[13] :

303 The semiconductor memory comprising: the sense amplifier in which the input terminal of one end is connected to the output end of the respective first amplified and the second pre-amplifier means, and the first and the second pre-amplifier means the information of the memory cell for the information remembering the information and the first and the second global bitline, in which the respective first detected and the second number of probe simple fruit, and the detect information of the first and the second probe means are the information of the first bit line, in which the memory cell for the information is connected and the reference memory cell, accumulating the reference information which uses when judging the value of the information accumulated in the memory cell for the information and the second bit line, in which the reference memory cell is connected and the first and the second bit line delivered and the first and the second global bitline to the other end of the respective connected first and the second condenser means, and the first and the second condenser means.

Claim[14] :

312 The semiconductor memory of claim 13, wherein the corrected transposition configuration method setting the corrected transposition to the first and the second bit line, and the short circuit means short-circuiting the terminal of the sense amp side of the condenser means are included.

Claim[15] :

315 The semiconductor memory comprising: the redundancy information storage cell group, having a plurality of memory cells memorizing the redundancy information with the break down of the heredity thin film and the decode means which has the other memory cell which whether the cell group of the magnetism is a valid or not remembers the information is an invalidation on the redundancy information storage cell group; and can change the coding by using the write means writing the redundancy information in the redundancy information storage cell group and the readout means making out the redundancy information and the transmission method, transmitting the redundancy information read with the readout means with the redundancy decoder and the redundancy information transmitted with the transmission method.

Claim[16] :

320 The semiconductor memory of claim 15, wherein the redundancy information memorized in the redundancy information storage cell group is the redundancy information after being compacted; the redundancy information read with the readout means the decompression processing of the redundancy information is performed; and it is transmitted with the transmission method to the redundancy decoder.

Claim[17] :

323 The semiconductor memory comprising: the transmission method transmitting the readout means, reading the redundancy information storage device, in which the compacted redundancy information is stored and the redundancy information stored in the redundancy information storage device and the extension treatment means, extending the redundancy information read with the readout means and the redundancy information extended with the extension treatment means with the redundancy decode means.

Claim[18] :

327

The semiconductor IC comprising: the control means which changes the configuration of the logic circuit block based on the logic circuit block, changing the circuit configuration and the circuit configuration information storage means, which the circuit configuration information of the logic circuit block is stored and the internal information storage means, which the internal information of the logic circuit block is stored and the circuit configuration information stored in the circuit configuration information storage means; and performs data

processing based on the internal information stored in the internal information storage means at least as the whole.

Claim[19] :

331 The semiconductor IC of claim 18, wherein the logic circuit block includes the common register performing the transfer of the information between 2 logic circuit blocks.

Claim[20] :

334 The semiconductor IC of claim 18, wherein the logic circuit block a plurality of is included; and the transfer timing of the circuit configuration information stored in the circuit configuration information storage means crosses each other in a plurality of logic circuit blocks.

Claim[21] :

337 The semiconductor IC comprising: the control means which memorizes the connection information of the wiring by the switching circuit, which selectively electrically connects a plurality of unit logics, changing a function and a plurality of wiring channels, intersecting with an plurality of input-output lead-out wirings extended from a plurality of unit logics and plurality of input-output lead-out wirings and plurality of wiring channels and switching circuit and channel with plural species; and it selects as the memory information of the middle one and controls the switching circuit.

Claim[22] :

341 The semiconductor IC, wherein in *** switch which includes the switch for connecting 2 wirings; and goes with the wiring, MOSFET for the condenser, in which a source and drain are connected to 2 wirings between the gate of the respective connected *** MOSFET, and *** MOSFET and fixed electric potential and the load in which the gate of *** MOSFET and load wiring and source and drain are connected and source is connected to the gate of MOSFET for the load; it has MOSFET for the CELP boot in which a drain is connected to the load start signal line; and the gate of MOSFET for the CELP boot is connected to the other fixed electric potential.

Claim[23] :

348 The semiconductor IC of claim 21, wherein in the switching circuit, MOSFET for the condenser, in which a source and drain are connected to 2 wirings 2 wirings 2 wirings between the gate of the respective connected *** MOSFET, and *** MOSFET and fixed electric potential and the load in which the gate of *** MOSFET and load wiring and source and drain are connected and source is connected to the gate of MOSFET for the load; it has MOSFET for the CELP boot in which a drain is connected to the load start signal line; and the gate of MOSFET for the CELP boot is connected to the other fixed electric potential.

Claim[24] :

357 The semiconductor memory that has data handling function, semiconductor memory comprising: data processing block which reads a plurality of datas of the first area, in which a plurality of datas is stored and the second part, which it is possible to store data and the first area; it collects these datas and it processes; and writes the process result in the second part.

Claim[25] :

360 The semiconductor memory that has data handling function, semiconductor memory comprising: data processing block which makes out data memorized in the first memory array, having a plurality of memory cells connected to a plurality of word lines and the second memory array, having a plurality of memory cells connected to a plurality of word lines and the memory cell connected to the word line of the fixed number from the first memory array; it collects these datas and it processes; and writes the process result in the memory cell connected to the word line of the fixed number of the second memory array.

Claim[26] :

363 The semiconductor memory having data handling function of claim 24, wherein data processing block compresses data read.

Claim[27] :

365 The semiconductor memory having data handling function of claim 25, wherein data processing block compresses data read.

Claim[28] :

367 The semiconductor memory having data handling function of claim 24, wherein data processing block extension-processes data read.

Claim[29] :

369 The semiconductor memory having data handling function of claim 25, wherein data processing block

extension -processes data read.

Claim [30] :

371 The semiconductor memory having data handling function, wherein: the data processing block dynamic makes out data group to process as described above and processing specification information; it processes data group processed as described above based on the treatment means information; and processing specification information store the process result to the third memory cell group; the first memory cell group is connected to the first word line group and data processing specification information of data processing block is stored; and the third memory cell group is connected to the third word late king and stores the process result.

Claim [31] :

377 The semiconductor memory having data handling function of claim 30, wherein data processing block includes the reconfigurable logic canning be programmed the ash.